1. (Currently Amended) A storage device for a multibus architecture, comprising:

at least one memory that stores information;

a memory connection having a port that is connected to the at least one memory and is selectively connected to one of a plurality of buses within the multibus architecture, at least one data line that communicates with the memory connection and the one of the plurality of buses to provide information to the memory connection to control the memory; ~~and~~

a switching device that selectively connects the memory connection to one of the plurality of buses to transmit information between the one of the plurality of buses and the memory; and

an analyzer that analyzes addresses on address lines which form a part of at least one of the plurality of buses for determining a selective access to the at least one memory by one of the plurality of buses, where the analyzer comprises an access control device that switches the switching device and a comparator that compares an address on one of the plurality of buses with a memory address of the at least one memory and controls the access control device to control the switching device as a function of the result of the comparison.

2. (Previously Presented) The storage device of claim 1, further comprising:

a logic device connected with an interrupt line that transmits an interrupt signal on the interrupt line from the logic device to a processor, where the interrupt signal interrupts operation of the processor for one clock cycle whenever a memory access is to be effected by the memory to two of the plurality of buses within two successive clock cycles.

3. (Cancelled)

4. (Currently Amended) The storage device of claim ~~3~~1, where the analyzer analyzes a part of the addresses and switches and assigns a memory access for address segments smaller than a word width of one of the plurality of buses having the addresses.

5. (Currently Amended) The storage device of claim 1~~3~~, further comprising an adjustable separator device that stores a memory address of the at least one memory for analysis by the analyzer.

6. (Cancelled)

7. (Currently Amended) The storage device of claim 1~~3~~, where the analyzer further comprises a modifier that processes different types of information applied to the modifier, where each one of the plurality of buses is selectively connected by the switching device to the modifier.

8. (Previously Presented) The storage device of claim 1, further comprising a logic device that provides a block loss signal on a signal line to a processor in response to a deviation from an executed data transfer during an access to the at least one memory.

9. (Previously Presented) The storage device of claim 1, where the at least one memory stores information that comprises data.

10. (Previously Presented) The storage device of claim 1, where the at least one memory stores information that comprises addresses.

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (Currently Amended) A storage device for use with a bus architecture having a plurality of buses including address, data and control information transmitted on the plurality of buses, the storage device comprising:

a memory;

a switching device that selectively connects the memory with one of the plurality of buses to transmit information on the selected one of the plurality of buses to the memory;

a logic device that provides an interrupt signal on a line to a processor to interrupt operation of the processor whenever an access to the memory is desired by at least one of the plurality of buses; and

an analyzer that analyzes an address on address lines that form a portion of at least one of the plurality of buses, where the analyzer controls the switching device to selectively connect one of the plurality of buses to the memory depending on the address that is analyzed by the analyzer, where the analyzer further comprises an access control device that switches the switching device and at least one comparator that compares an address on one of the plurality of buses with a memory address of the memory and controls the access control device to control the switching device as a function of the result of the comparison.

21. (Currently Amended) The storage device of claim 20, further comprising a separator device that stores the~~an~~ address ~~of the memory~~ for analysis by the analyzer.

22. (Cancelled)

23. (Cancelled)

24. (Currently Amended) The storage device of claim 20, where the analyzer further comprises a modifier that determines the type of information that is provided to the memory for storage thereby.

25. (Currently Amended) The storage device of claim 24, where the modifier determines the type of information that is provided on the one of the plurality of buses that is connected with the memory by the switching device.

26. (Currently Amended) The storage device of claim 20, where the memory further comprises a memory connection that facilitates connection of the memory to the ~~information on the~~ one of the plurality of buses selectively connected to the memory ~~connection~~ by the switching device.

27. (Currently Amended) The storage device of claim 20, where the information stored by the memory comprises data.

28. (Currently Amended) The storage device of claim 20, where the logic device provides a block loss signal on a line to ~~a~~ the processor in response to a deviation from an executed data transfer during an access to the memory.

29. (Currently Amended) A method for storing data in a memory storage device for use with a bus architecture having a plurality of buses, the method comprising:

selectively connecting the memory storage device with one of the plurality of buses to transmit the information on the selected one of the plurality of buses to the memory storage device;

interrupting operation of a processor whenever an access to the memory storage device is desired by at least one of the plurality of buses; and

analyzing an address on address lines that form a portion of at least one of the plurality of buses and by controlling the selective connection of one of the plurality of buses to the memory storage device depending on the address analyzed by the analyzer, where the step of analyzing further comprises the step of controlling access to the memory storage device by comparing an address on one of the plurality of buses with a memory address of the memory storage device and selectively connecting the memory storage device with one of the plurality of buses as a function of the comparison step.

30.(New) A storage device for a multibus architecture, comprising

a memory device to store data, addresses and control information;

a first bus, a second bus and a third bus each having data lines to transmit the data, addresses and control information between the first, second and third buses and the memory device via a memory connection to control the memory device;

a switching device that selectively connects the memory connection to a selected one of the first, second and third buses for memory access to effect transmission of the data, addresses or control information via the selected first, second or third bus;

an analyzer connected on the input side of the memory device for analyzing addresses on the address lines and switching the switching device to one of the first, second or third buses; and

programmable separator device that stores a memory address of the memory device for analysis by the analyzer.